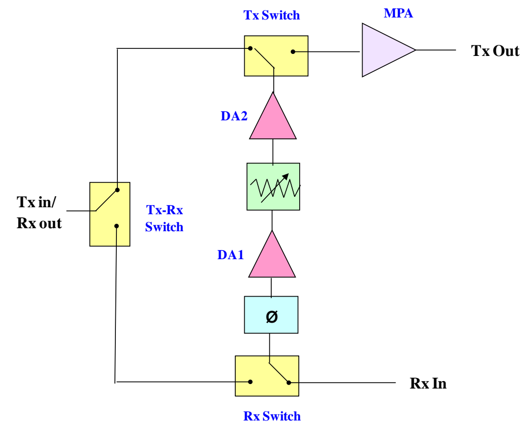
9 - 10 GHz GaAs MMIC Core Chip

Features

- **Frequency Range: 9GHz – 10GHz**
- **Tx Small Signal Gain: 28dB**
- **Rx Small Signal Gain: 4dB**
- **Tx Output P1dB : 22dBm**
- **Tx Output Psat : 23dBm**
- **Input Return Loss < 12 dB**
- **Output Return Loss < 12 dB**
- **Phase Shifter Range : 6 Bit, 5.625° step**
- **Attenuator Range : 6 Bit, 0.5dB step**
- **0.5 µm InGaAs pHEMT Technology**
- **Chip dimension: 5.3 x 5.3 x 0.1 mm**

Functional Diagram



Typical Applications

- **RADAR**
- **Military & space**
- **VSAT**

Description

The ASL6000 is a multi-functional Transmit / Receive 3 port core chip. It is designed for applications operating within the 9 GHz to 10 GHz range. This core chip consists of integrated transmit/receive switches, 6-bit phase shifter, 6-bit attenuator, driver amplifier and medium power amplifier. The digital control logic allows fast phase shifter and attenuator changes. The RF ports of the core chip across RX path (RXIN and TXIN/RXOUT) are DC coupled ports. The chip has surface passivation to protect the internal circuit. It also has backside via holes and gold metallization to allow either a conductive epoxy or eutectic solder die attach process. This device is well suited for phased array radar applications.

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Absolute Maximum Ratings[1]:

Parameter	Absolute Maximum	Units
Supply Voltage (Vd)	6	V
Gate Supply (-5V)	-6 to -4	V
Control Logic Supply	0 to +5.5	V
RF input at Tx_{in} Port	16 @ 85 °C	dBm
RF input at Rx_{in} Port	17 @ 85 °C	dBm
Supply current in Tx Mode	+380	mA
Supply current in Rx Mode	+150	mA
Operating temperature	-50 to +85	°C
Storage Temperature	-65 to +150	°C

Test fixture data:

VdDA1 = VdDA2 = VdMPA = 5V ; Total Current = 107mA, T_A = 25 °C (Pulse duty = 10%)

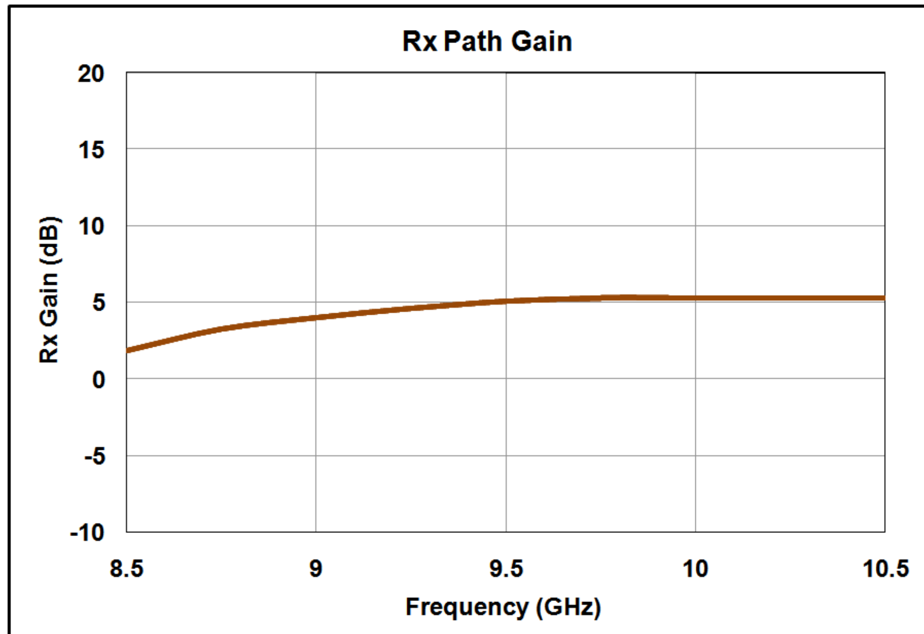
Parameter	Typical Value	Units
Frequency Range	9.0-10.0	GHz
Receive Small Signal Gain	4.0	dB
Transmit Small Signal Gain	28	dB
Transmit Large Signal Gain (@ Pin = 0dBm)	23	dB
Input / Output Return Losses	12	dB
Receive Output Power for 1dB Compression Point	13.5	dBm
Receive Output Third Order Intercept Point	24	dBm
Transmit Output Power for 1dB Compression Point	22	dBm
Transmit Output Saturated Power	23	dBm
Phase Shifter Range (6 Bit, 64 states, 5.625° step)	0 – 355	deg
RMS Phase Error	3	deg
Attenuation Range (6 Bit, 64 states, 0.5dB step)	0 – 31.5	dB
RMS Attenuation Error	0.7	dB
Tx/Rx Switch Isolation	< -57	dB
Supply Voltages	+5, -5, -1	V
Supply Current (@ 10% Duty Cycle in Tx mode)	~ 107	mA
Control Voltage	TTL Compatible	V
Chip Size	5.2 x 5.4	mm

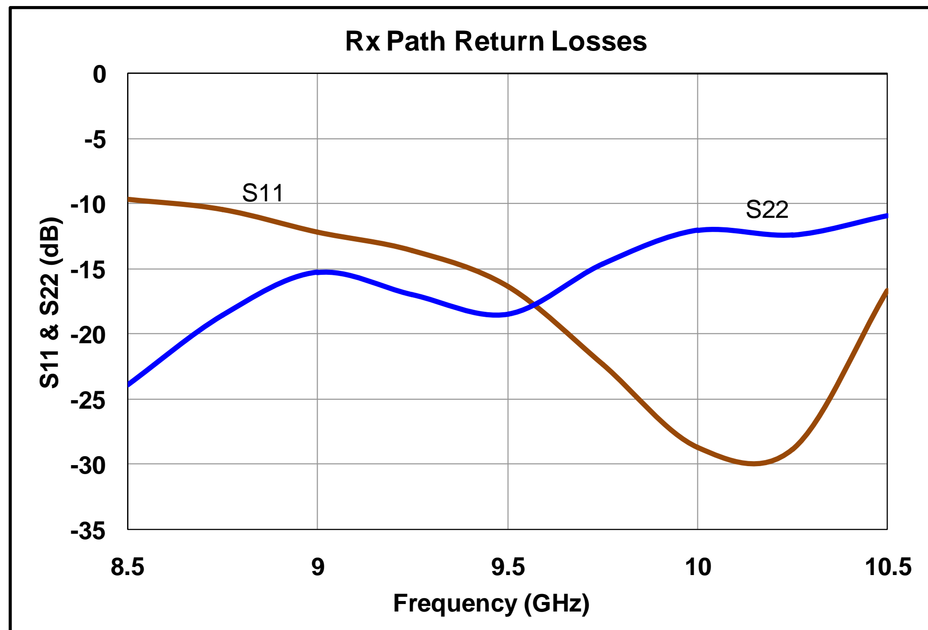
Note:

1. Electrical specifications are measured in a text fixture.

Test fixture data in Rx Path (Tx/Rx Control = 0V):

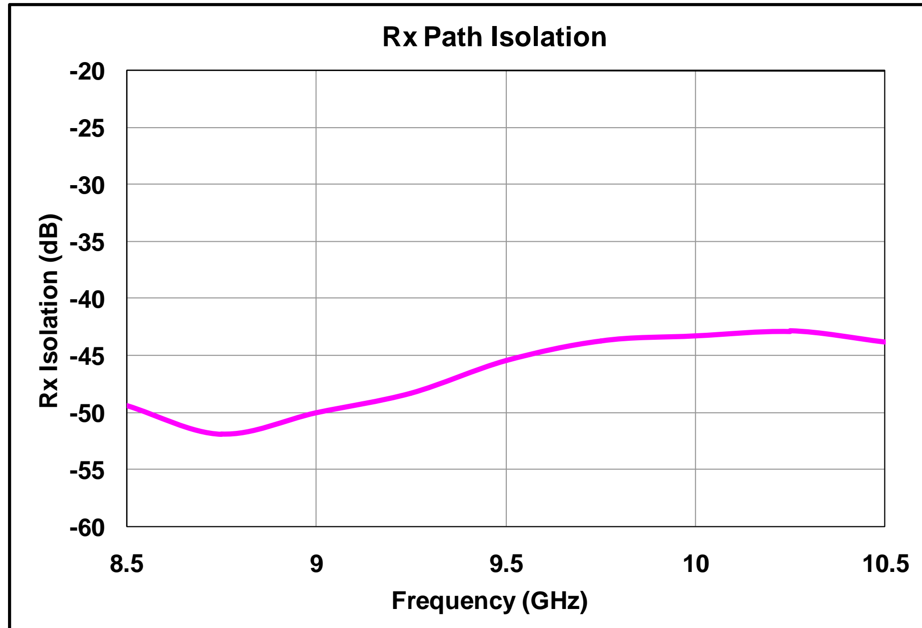
VdDA1 = VdDA2 = 5V ; Total Current = 90mA, T_A = 25 °C

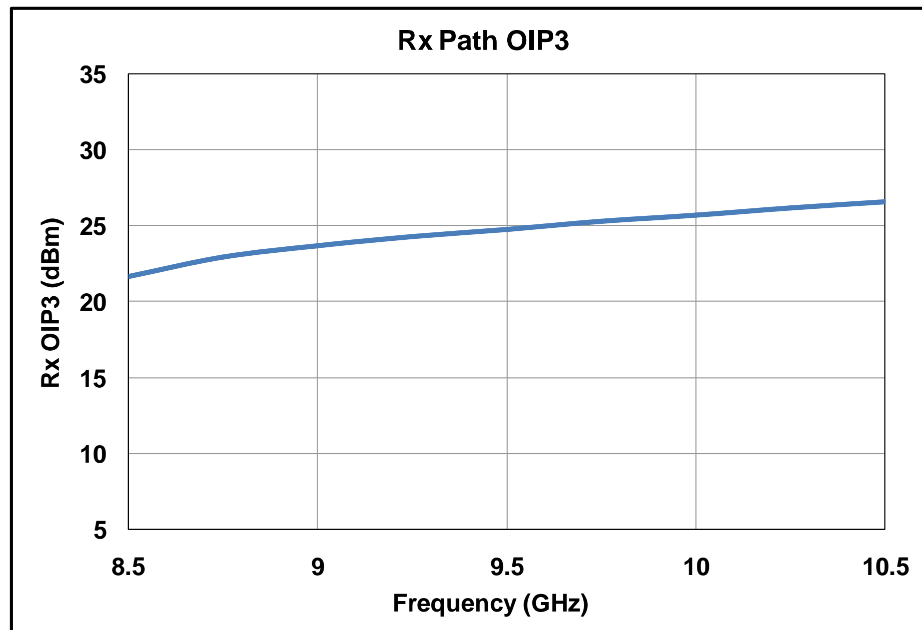




Test fixture data in Rx Path (Tx/Rx Control = 0V):

VdDA1 = VdDA2 = 5V ; Total Current = 90mA, T_A = 25 °C





Test fixture data in Rx Path (Tx/Rx Control = 0V):

VdDA1 = VdDA2 = 5V ; Total Current = 90mA, T_A = 25 °C

6 Bit Digital Phase Shifter Performance (only prime states):

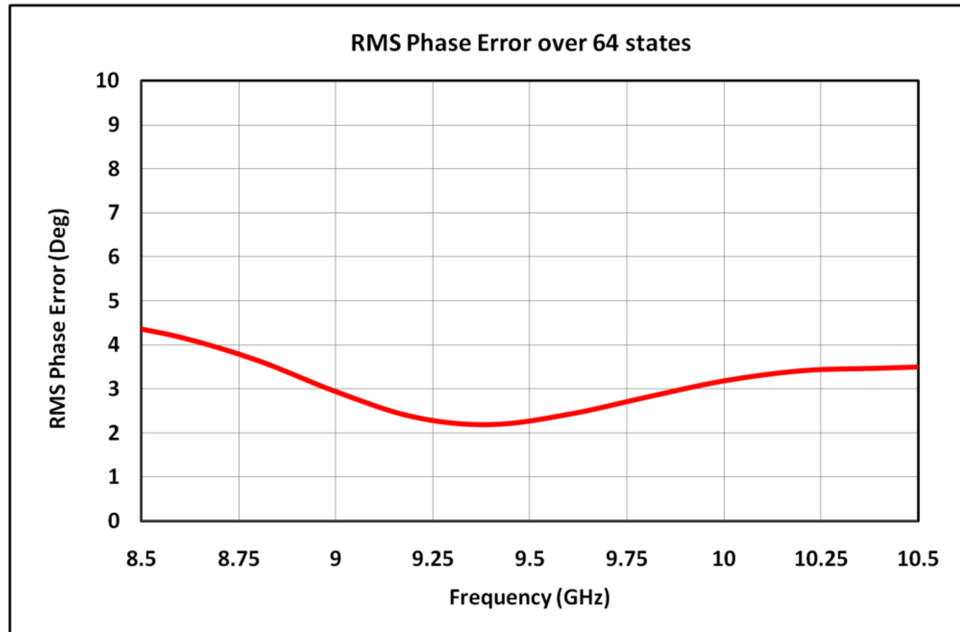
Bit / State (in Degree)	Frequency (GHz)		
	9	**9.5**	**10**
5.625	6.2	6.4	6.8
11.25	12.1	12.3	12.8
22.5	20.5	20.6	20.1
45	46.3	45	45.5
90	90.6	88.5	88.9
180	176.3	178.5	179.3

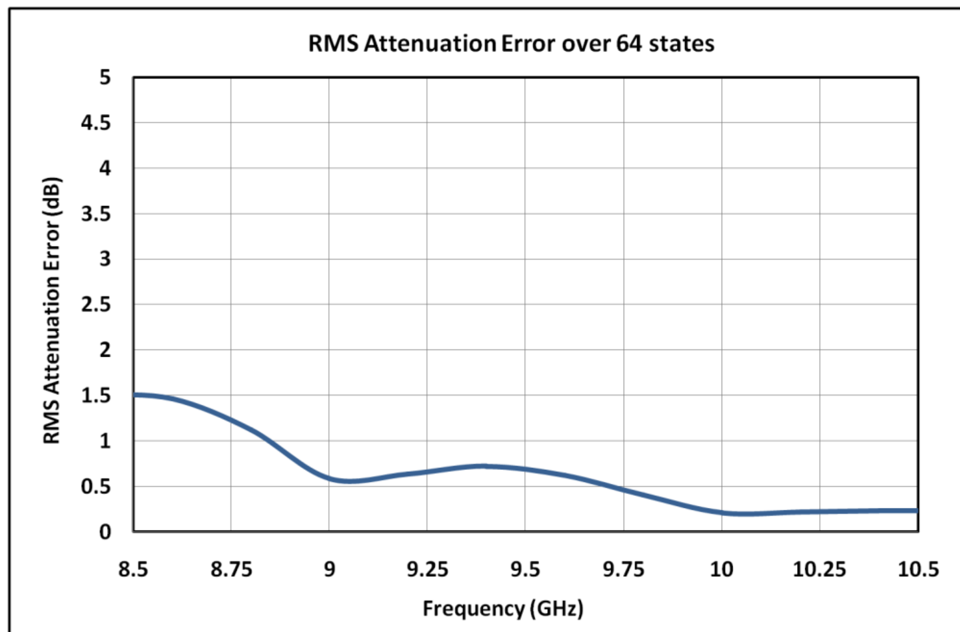
6 Bit Digital Attenuator Performance (only prime states):

Bit / State (dB)	Frequency (GHz)		
	9	**9.5**	**10**
0.5	0.43	0.42	0.44
1	0.92	0.93	0.95
2	2.1	2.05	2.14
4	4.02	3.95	4.12
8	7.8	8.15	8.2
16	16.05	16.75	16.3

Test fixture data in Rx Path (Tx/Rx Control = 0V):

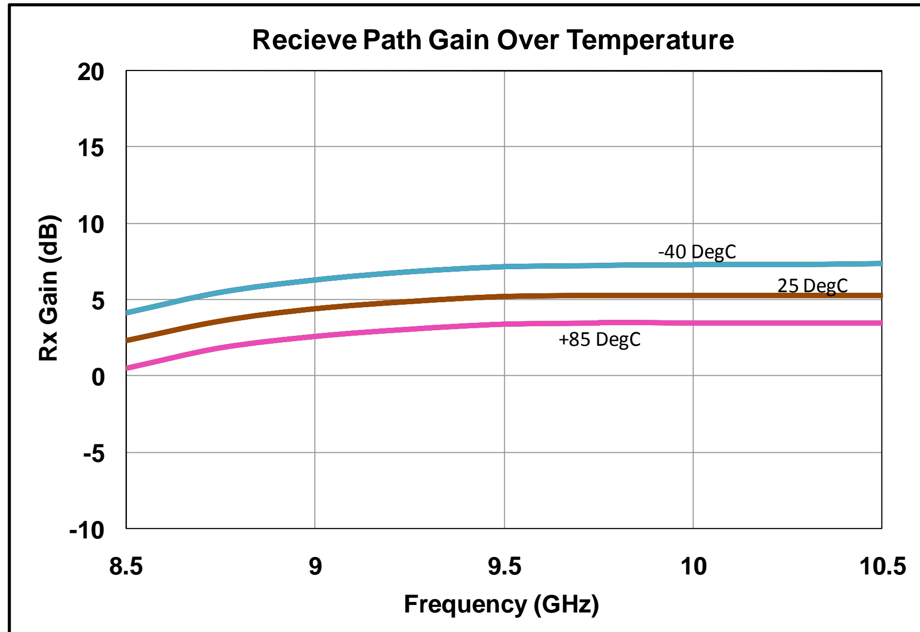
VdDA1 = VdDA2 = 5V ; Total Current = 90mA, T_A = 25 °C

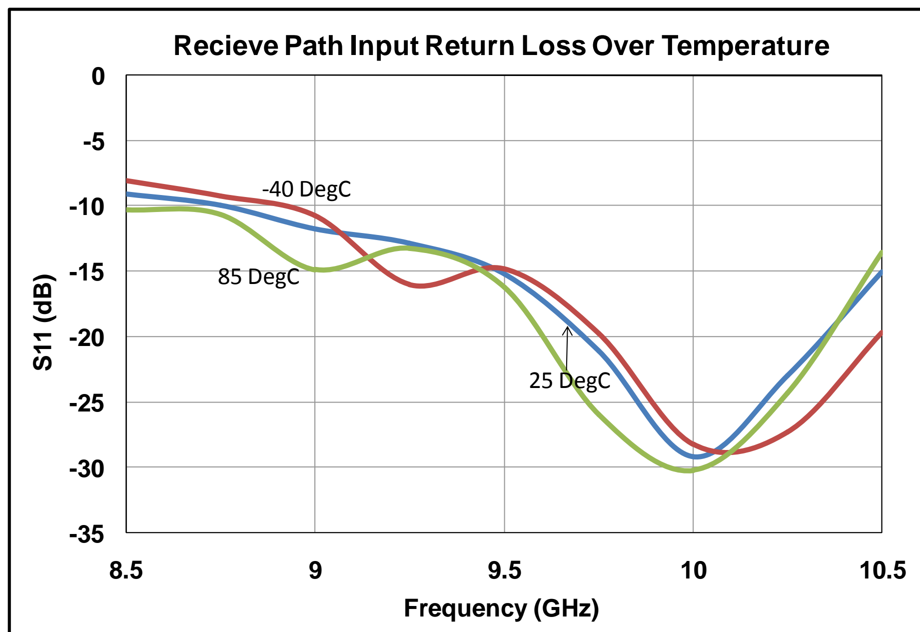




Temperature data in Rx Path (Tx/Rx Control = 0V):

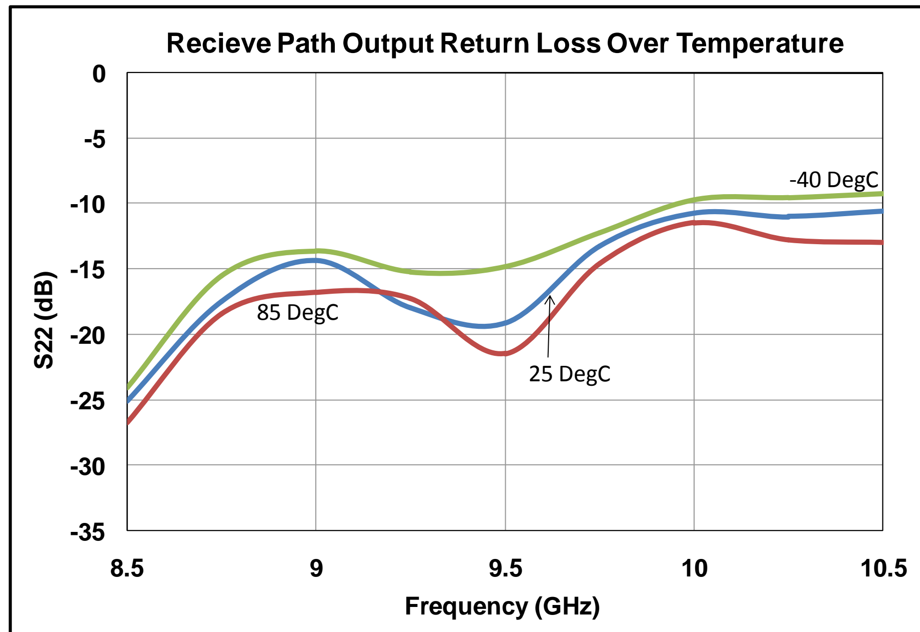
VdDA1 = VdDA2 = 5V ; Total Current = 90mA, T_A = 25 °C





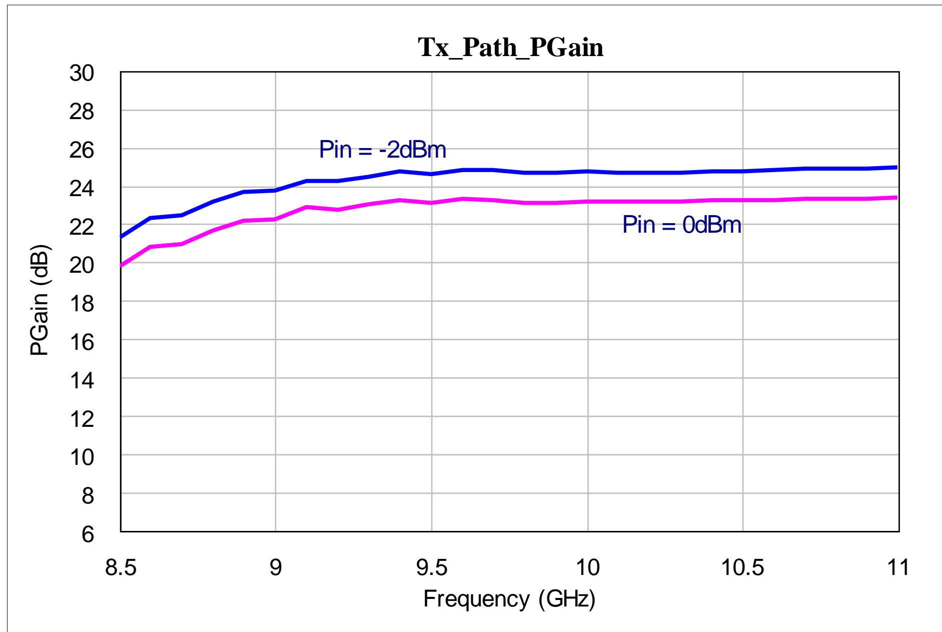
Temperature data in Rx Path (Tx/Rx Control = 0V):

VdDA1 = VdDA2 = 5V ; Total Current = 90mA, T_A = 25 °C

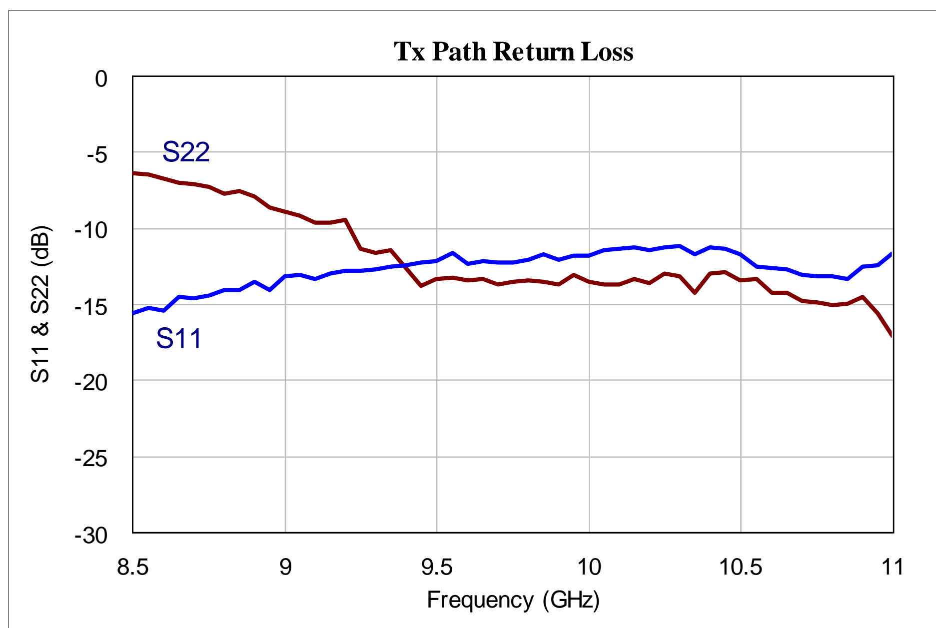


Test fixture data in Tx Path (Tx/Rx Control = 3.3V); Pulse Duty = 10%:

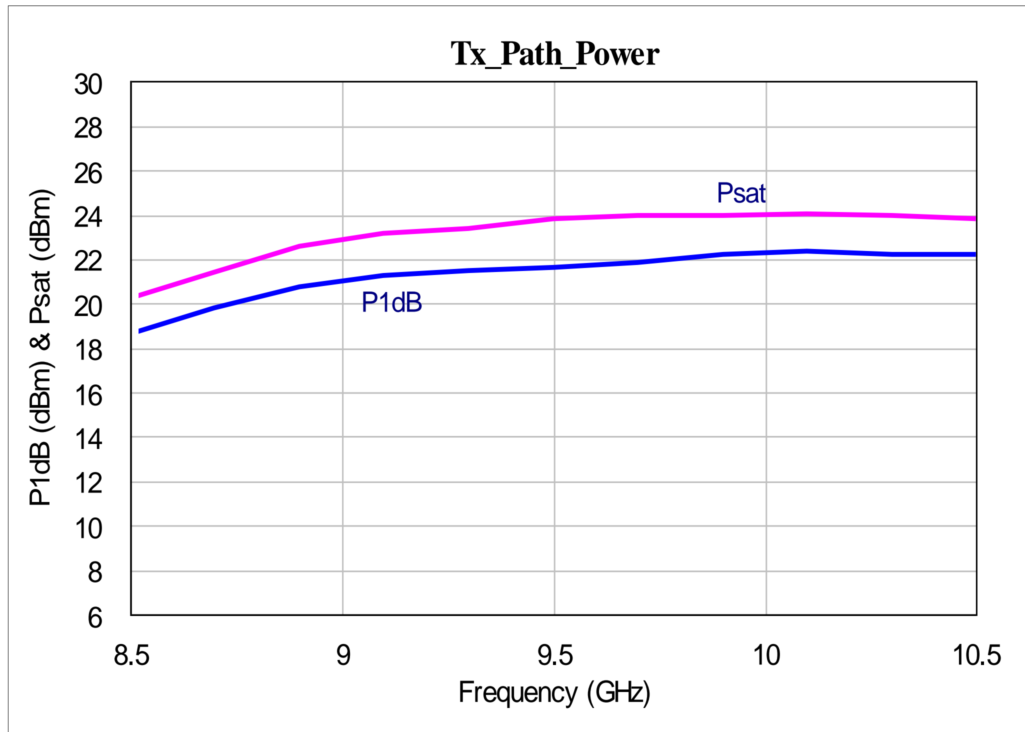
VdDA1 = VdDA2 = VdMPA = 5V ; Total Current = 107mA, T_A = 25 °C



Tx Path Gain over Input Power

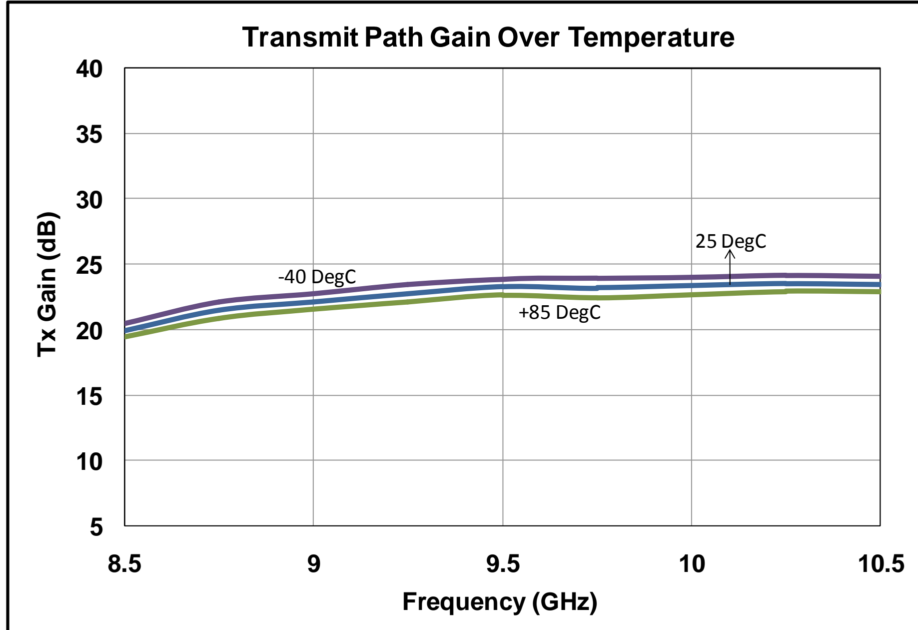


Test fixture data in TX Path (Tx/Rx Control = 3.3V); Pulse Duty = 10%:
VdDA1 = VdDA2 = VdMPA = 5V ; Total Current = 107mA, T_A = 25 °C

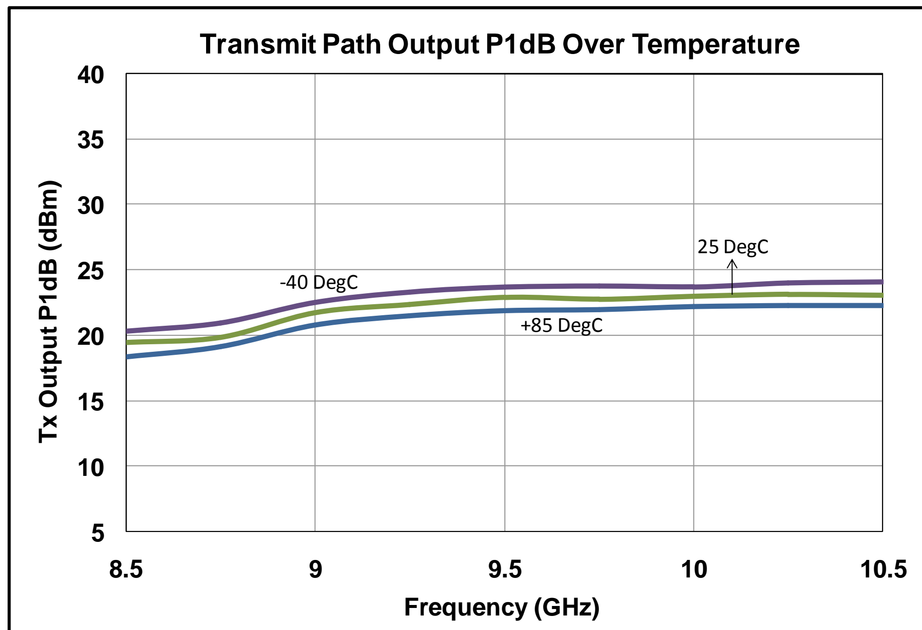


Temperature data in TX Path (Tx/Rx Control = 3.3V); Pulse Duty = 10%:

VdDA1 = VdDA2 = VdMPA = 5V ; Total Current = 107mA, T_A = 25 °C

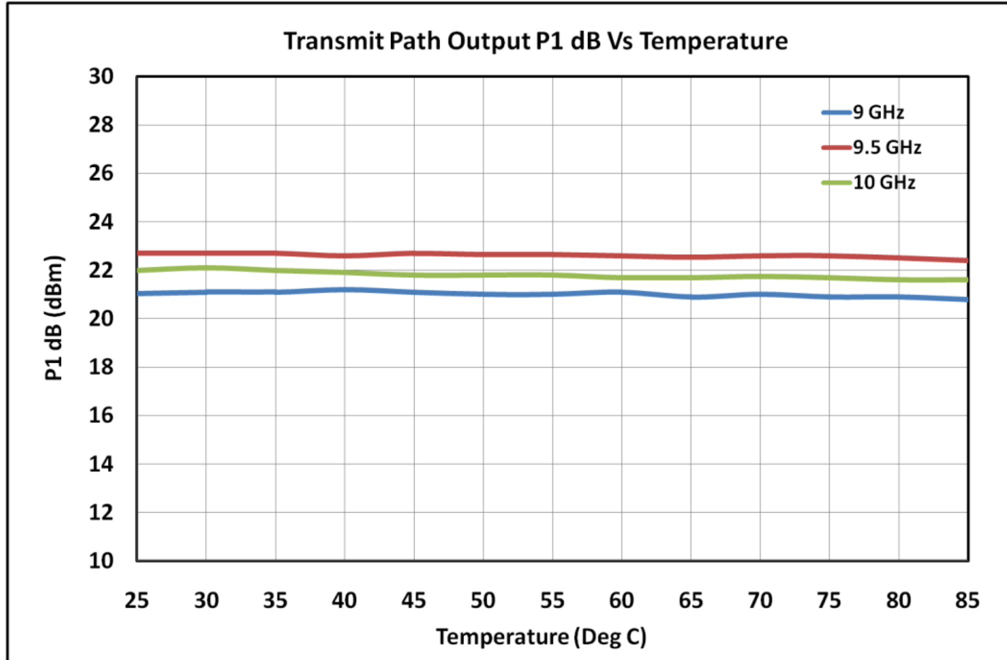


Tx Gain over Temperature @ Pin = 0dBm

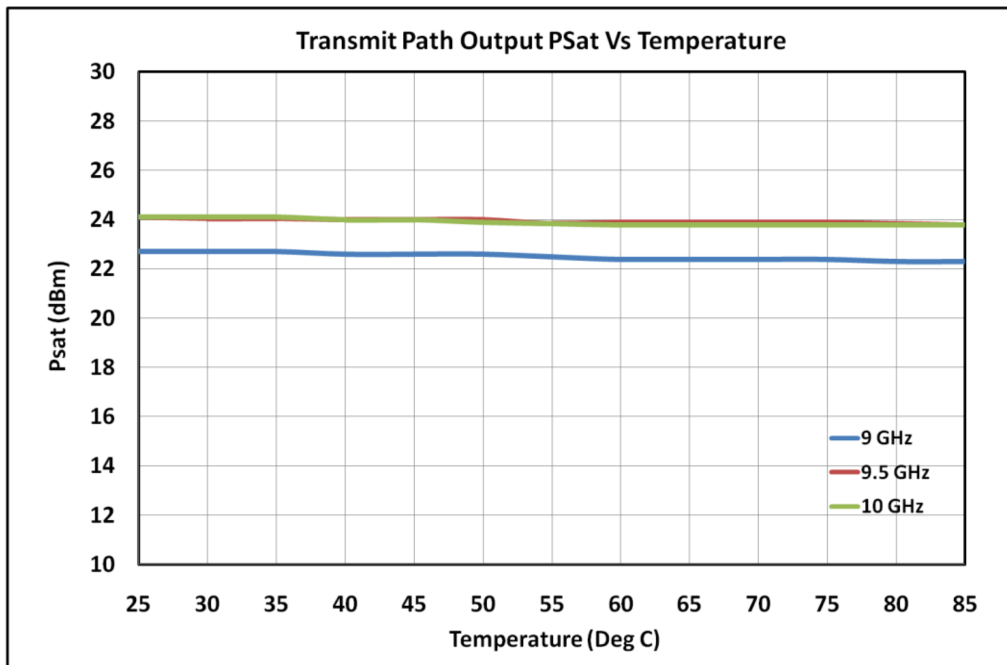


Temperature data in TX Path (Tx/Rx Control = 3.3V); Pulse Duty = 10%:

VdDA1 = VdDA2 = VdMPA = 5V ; Total Current = 107mA, T_A = 25 °C

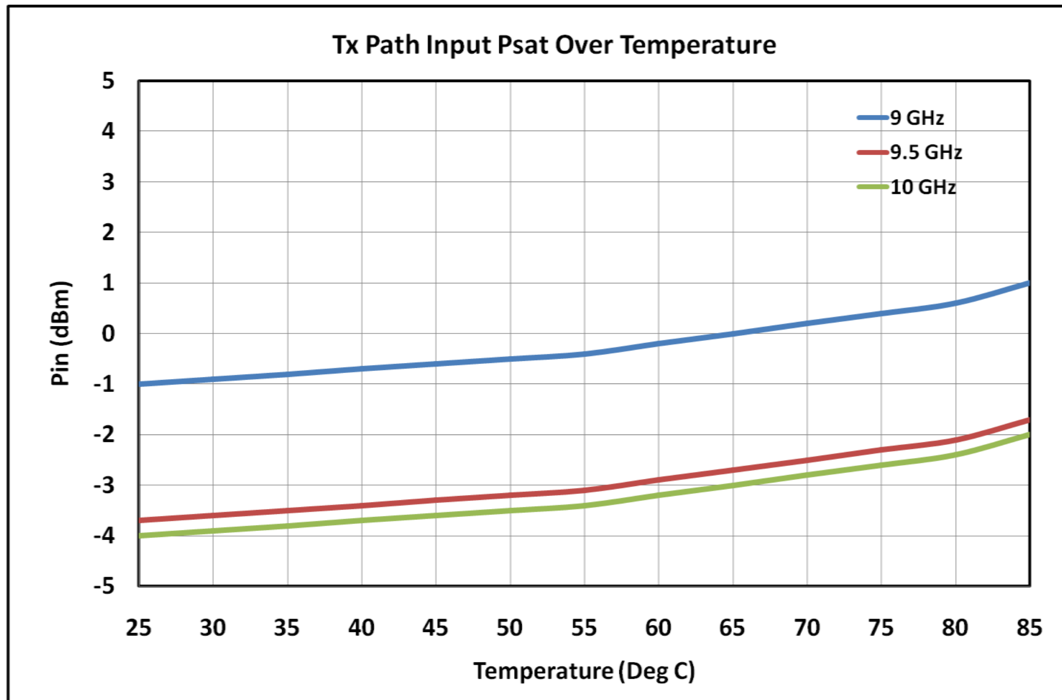


Tx Path Output P1dB plotted with Temperature on X-axis



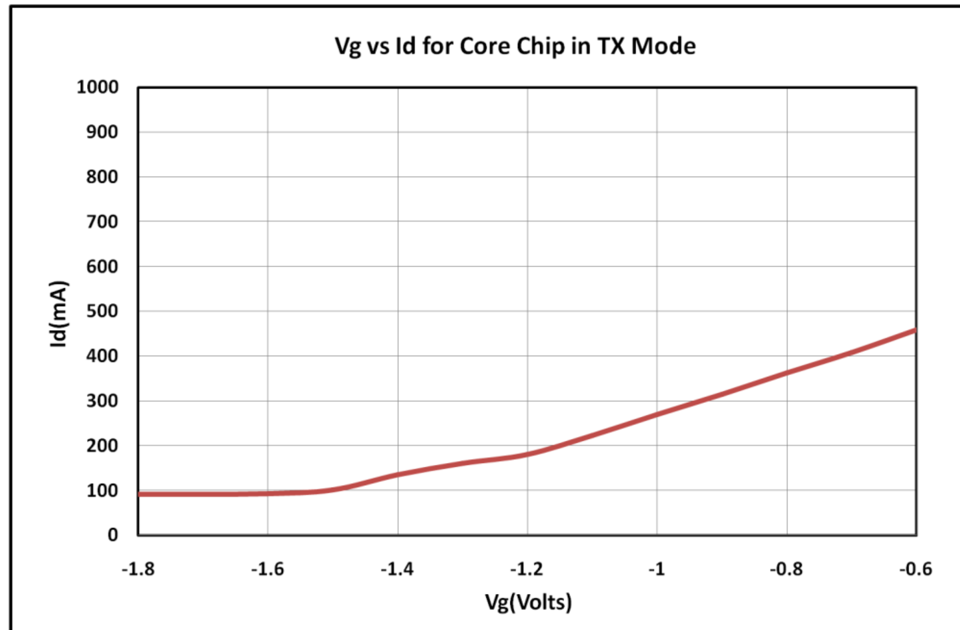
Tx Path Output Psat plotted with Temperature on X-axis

Temperature data in TX Path (Tx/Rx Control = 3.3V); Pulse Duty = 10%:
VdDA1 = VdDA2 = VdMPA = 5V ; Total Current = 107mA, T_A = 25 °C



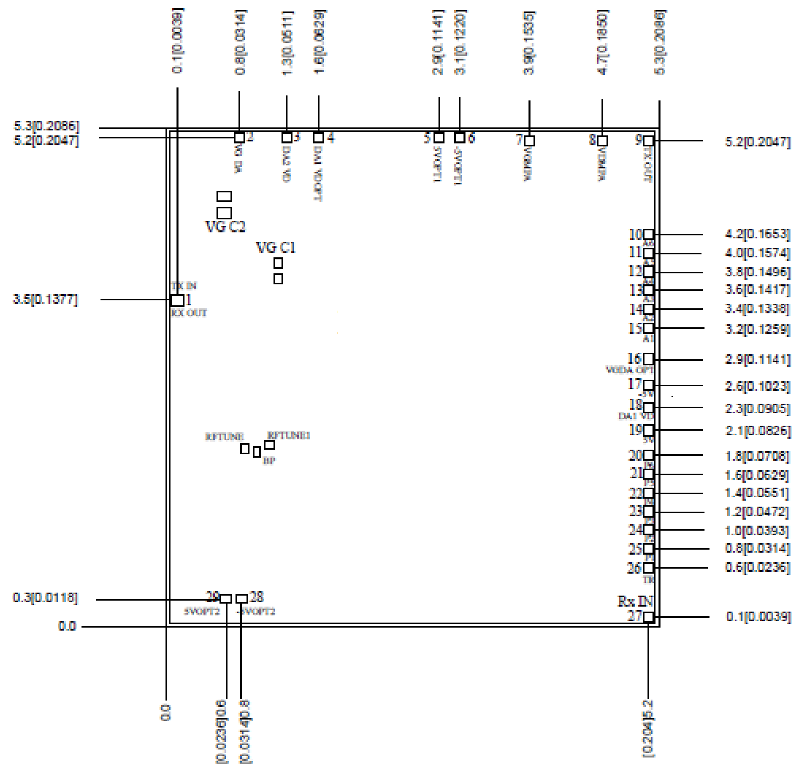
Tx Path Input Power of Core Chip Corresponding to Saturated
Output Power Plotted with Temperature on X-axis

Temperature data in TX Path (Tx/Rx Control = 3.3V); Pulse Duty = 10%:
VdDA1 = VdDA2 = VdMPA = 5V ; Total Current = 107mA, T_A = 25 °C



Current variation of core chip in Tx mode over different gate voltages

Mechanical Characteristics:



Units: Millimeters [Inches]

All RF and DC bond pads are 100µm x 100µm

Note:

1. **Pad no. 1 : T_XIN / R_XOUT**
2. **Pad no. 3 : DA2 Vd (Drain Voltage of DA2) = +5 V**
3. **Pad no. 19 : +5V (+5V Supply Voltage for Control Circuits)**
4. **Pad no. 6 : -5VOPT1 (-5V Supply Voltage for Control Circuits)**
5. **Pad no. 7 : VgMPA (Gate Voltage of MPA) = -1 V (Typ)**
6. **Pad no. 8 : VdMPA (Drain Voltage of MPA) = +5 V**
7. **Pad no. 9 : $T_X$out (Output of the Transmit Path)**
8. **Pad no. 10-15 : A1-A6 (Attenuator controls) = (3.3- 5V)**
9. **Pad no. 18 : DA1 Vd (Drain Voltage of DA1) = +5 V**
10. **Pad no. 20-25 : P6-P1 (Phase shifter controls) = (3.3 – 5V)**
11. **Pad no. 26 : T_X/R_X (T_X/R_X Switch) = (3.3 – 5V)**
12. **Pad no. 27 : R_X IN (Input of the Receive Path)**
13. **Pad no. 4 : DA1 VdOPT has to be connected to 100pF Single Layer bypass Capacitor through 50ohm Thin film resistor (in series) in order to achieve better RMS attenuation error.**

All other Bond Pads are NC (No Connection).

On Chip and Off Chip Tuning Provisions:

1. On chip Bond Pads ‘BP’ to ‘RFtune’ and ‘BP’ to ‘RFtune1’ are to be shorted so as to achieve better return loss across the common port (Txin/Rxout) of the core chip.

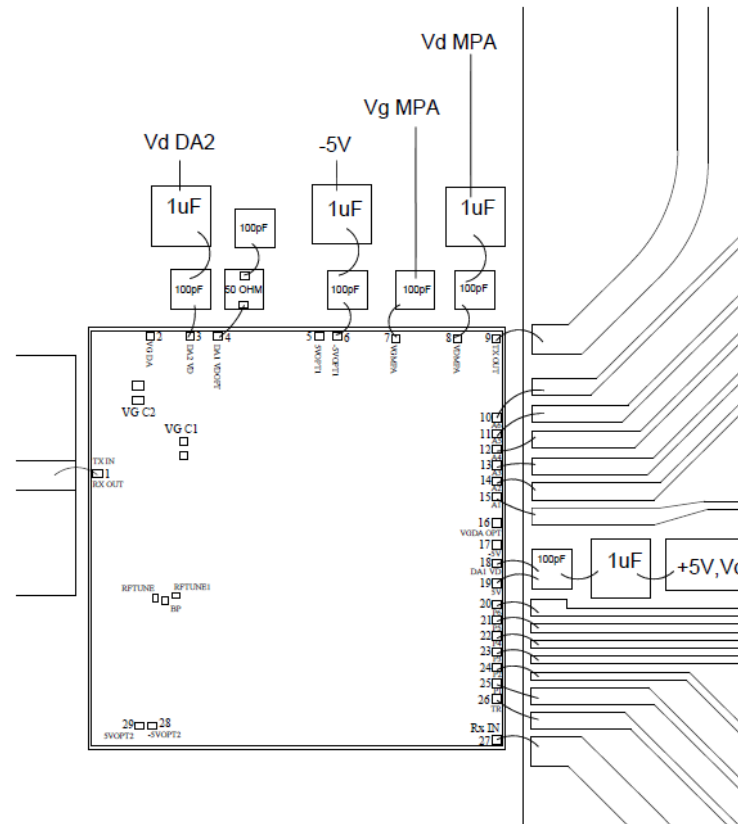
2. By shorting two on chip Bond Pads shown at “Vgc1” of the core chip, the gate voltage across common path amplifiers changes from -0.9V to -1.1V, there by the overall current of the core chip reduces by 34mA and consequently gain across Tx path and Rx path reduces by 2dB.

3. By shorting two on chip Bond Pads shown at “Vgc2” of the core chip, the gate voltage across common path amplifiers changes from -0.9V to -0.8V, there by the overall current of core chip increases by 18mA and consequently gain across Tx path and Rx path increases by 1dB.

4. If the 5V drain bias supply is applied to Pad no.4 (DA1VdOPT) instead of Pad no.18 (DA1Vd), the small signal positive gain slope across Tx path and Rx path increases to 2dB. Therefore, it is recommended to apply the drain bias supply (5V) to Pad no.18 for better gain slope across Tx path and Rx path of the core chip.

5. At Pad no.4 (DA1VdOPT) DA1 VdOPT has to be connected to 100pF Single Layer bypass Capacitor through a 50 ohm Thin film resistor (in series) in order to achieve better RMS attenuation error (as shown in assembly diagram).

Recommended Assembly Diagram:



Note:

1. Two 1 mil (0.0254mm) bond wires of minimum length should be used for RF input and output.
2. Two 1 mil (0.0254mm) bond wires of minimum length should be used from chip bond pad to 100pF Single Layer Bypass Capacitor.
3. Input and output 50 ohm lines are on 5 mil substrate.
4. For reliable operation, DC decoupling capacitor is recommended to be used at pad no.27 (RXIN) and pad no.1 (TXIN/RXOUT).
5. Use high thermal conductive material for die mounting in order to achieve higher MTBF of the device.

Die attach: For Epoxy attachment, use of a two-component conductive epoxy is recommended. An epoxy fillet should be visible around the total die periphery. If Eutectic attachment is preferred, use of fluxless AuSn (80/20) 1-2 mil thick preform solder is recommended. Use of AuGe preform should be strictly avoided.

Wire bonding: For DC pad connections use either ball or wedge bonds. For best RF performance, use of 150 - 200µm length of wedge bonds is advised. Single Ball bonds of 250-300µm though acceptable, may cause a deviation in RF performance.

GaAs MMIC devices are susceptible to Electrostatic discharge. Proper precautions should be observed during handling, assembly & testing

All information and Specifications are subject to change without prior notice

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